Technical Training (TT) scholarship in High-Performance Computing
FAPESP Scholarships
(University of São Paulo, Brazil)

We are currently seeking three highly motivated and skilled Technical Training researchers to join our team and contribute to the thematic project "Trends in High-Performance Computing – From Resource Management to New Computer Architectures." The ideal candidates should have a strong Computer Science background and experience in High-Performance Computing applications. As a part of our team, the Technical Training researchers (two at level 4A and one at level 5) will focus on the project "Improving parallel applications in heterogeneous environments." If you believe you have the necessary skills and experience, we encourage you to apply for this position and help us advance in the field of HPC. The positions are open to candidates from all nationalities.

Description

At the beginning of the project "Trends in High-Performance Computing – From Resource Management to New Computer Architectures" (process 2019/26702-8, principal investigator Alfredo Goldman), we acquired eight FPGA boards. We will need to develop related tools and experiments on this machine. We are also in the process of acquiring a new parallel machine (150 K USD) for experiments.

An essential aspect of this work is adapting existing parallel applications to the project's context, which will serve as both examples of applications of interest and test cases while also facilitating the adoption of the project's results by groups interested in these applications.

To achieve this, we must assemble a team consisting of two Level IV-A Technical Training scholarship holders and one Level V Technical Training scholarship holder. As a result, we expect to make significant contributions to the parallelization of several problems with high computational demands.

Requirements

Technical Training IV-A (TT 4A) – 2 positions
Scholarship Amount: R$ 7,080.00 monthly

a. for candidates who are graduates in Computer Science or related fields;
b. with a minimum of four years of research experience or professional experience after graduation in a field related to the proposed Activity Plan; and
c. with a commitment of 16 to 40 hours per week (the scholarship amount paid will be proportional to the number of weekly hours) to support the research project activities.

The TT-IV-A fellows will work on modifying the code of existing applications to adapt them to the tools and techniques developed by the project researchers, testing them, and evaluating the results obtained together with the researchers on the FPGA machine.
The research and activities carried out by the fellows who make up the team for this project will contribute to the work of other researchers, such as undergraduate and graduate students and professors from the Computer Science department at IME-USP.

The development work will follow the most relevant practices of agile methodologies. Access to the Multi-User Equipments (EMUs) will allow quality and performance testing to be carried out regularly. Integrating development with the work of researchers will allow the publication of scientific papers describing the results obtained.

The expected results schedule includes a literature review in the HPC area, analysis and testing of the applications developed, writing of partial and final reports, participation in conferences, and publication of academic articles to disseminate the partial and final results. In this project, TT-IV-A scholarship recipients are expected to generate results such as parallelizing some real problems in the available architectures. The expected duration of the scholarship is 12 months, renewable for additional 12 months.

Technical Training V (TT-5) – 1 position
Scholarship Amount: R$ 9,320.00 monthly

a. for candidates who are graduates in Computer Science and related fields;
b. with a minimum of five years of research experience or professional experience after graduation, or with a doctorate, both in a field related to the proposed Activity Plan; and
c. with a commitment of 16 to 40 hours per week (the scholarship amount paid will be proportional to the number of weekly hours) to support the research project activities.
The TT-V fellow, as the team's senior developer, should guide and coordinate the work of the two TT-IV-A fellows, outlining methods and policies, as well as interacting with the group's researchers to define priorities and strategies to ensure the smooth running of the work.

In addition, he/she should also work on the development itself. His/her duties include:

- Choosing, together with the project's researchers, the main applications to be adopted in the development;
- Defining the strategies, methods, and metrics to be adopted by the fellows for the development process;
- Throughout the development process, discussing with the researchers the desirable improvements identified in the APIs and support libraries developed by the project to meet the needs of the application developers;
- Supporting the project's researchers in running experiments;
- Effectively changing the chosen applications to make use of the tools and techniques under investigation by the project;
- Assisting in the preparation of the EMU and FPGA machine manual.

The development work will follow the most relevant practices of agile methodologies. Access to the EMUs will allow quality and performance tests to be carried out regularly. Integrating development with the researchers' research will allow the publication of scientific papers describing the results obtained.

The expected results schedule includes a literature review in the HPC area, analysis and testing of the applications developed, writing of partial and final reports, participation in conferences, and publication of academic articles to disseminate the partial and final results. The expected duration of the scholarship is 12 months, renewable.

In this project, the TT-V scholarship holder is expected to generate results such as the parallelization of real applications on the two machines. Since much of the work to be developed consists of team software development (3 scholarship holders), TT5 must have greater experience and technical competence to manage the progress of the work and solve advanced technical issues.

What we offer

We offer a competitive FAPESP fellowship (R$ 9,320.00 for TT5 and R$ 7,080.00 for TT4A). Successful candidates will be supervised by Prof. Dr. Alfredo Goldman.

The Technical Training researchers will be based at the Department of Computer Science at the University of São Paulo, located in São Paulo city. This dynamic and collaborative environment offers numerous opportunities for professional development and research collaboration. The position is available immediately following the completion of the selection process.

How to Apply

To apply for the position, send the following documents in PDF format by email to gold@ime.usp.br with a copy to camila.ap@ime.usp.br:

• A cover letter explaining why you are a good fit for the project.

• Curricular Summary in the format requested by FAPESP.
Instructions for the elaboration of a Curricular Summary can be found here: https://fapesp.br/6351/instructions-for-the-elaboration-of-a-curricular-summary.

Application Deadline

The application deadline is 17 January 2025. The selection is expected to be finished around a month after the application deadline.